

FIG. 1 is a block diagram of a system for debugging a target device. The system includes a Debug Controller (1), a Discrimination Device (3), and a target device (2). The Debug Controller (1) is connected to the Discrimination Device (3) and the target device (2). The target device (2) includes a CPU (2-2), a Debug I/F (2-1), a PORT (2-3), a Send Circuit (2-4), a Shift Register (2-6), a Collate Detector (2-7), a Timer (2-8), and a Peripheral (2-12). The system also includes an OSC (Oscillator) and a DRSTZ901 (Reset Zener Diode).

FIG. 1

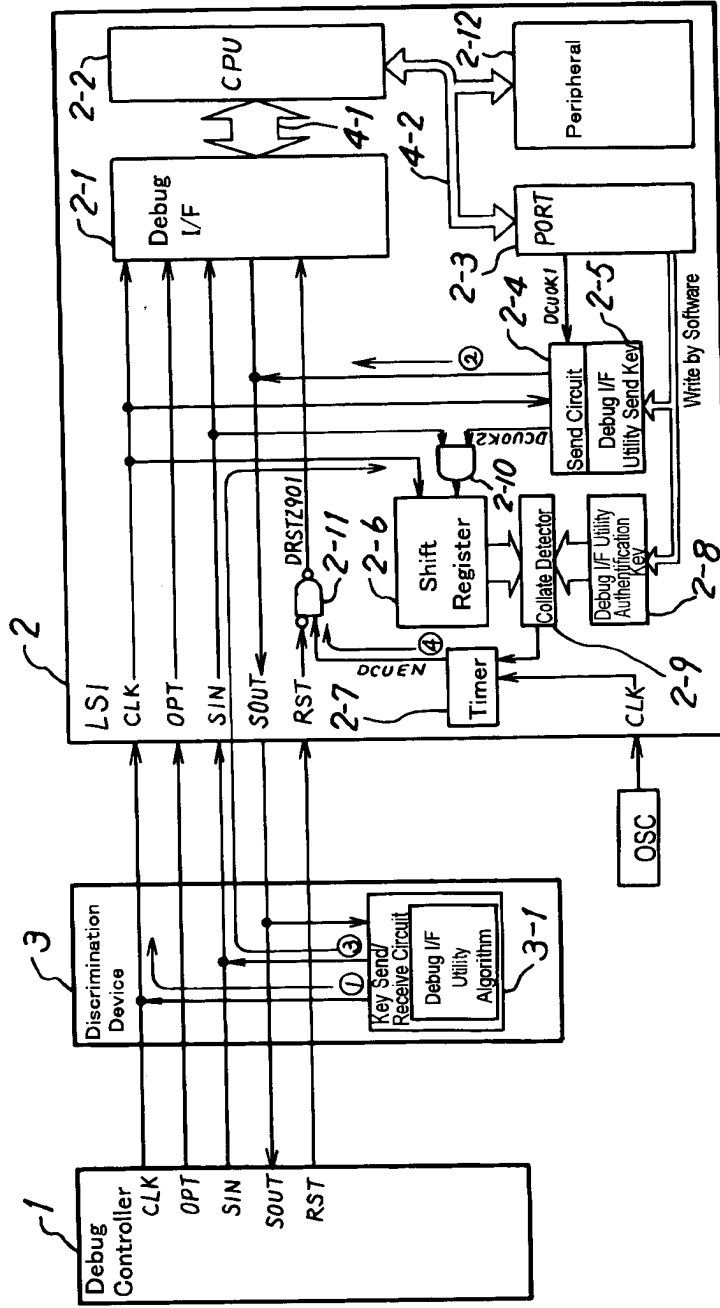


FIG. 2

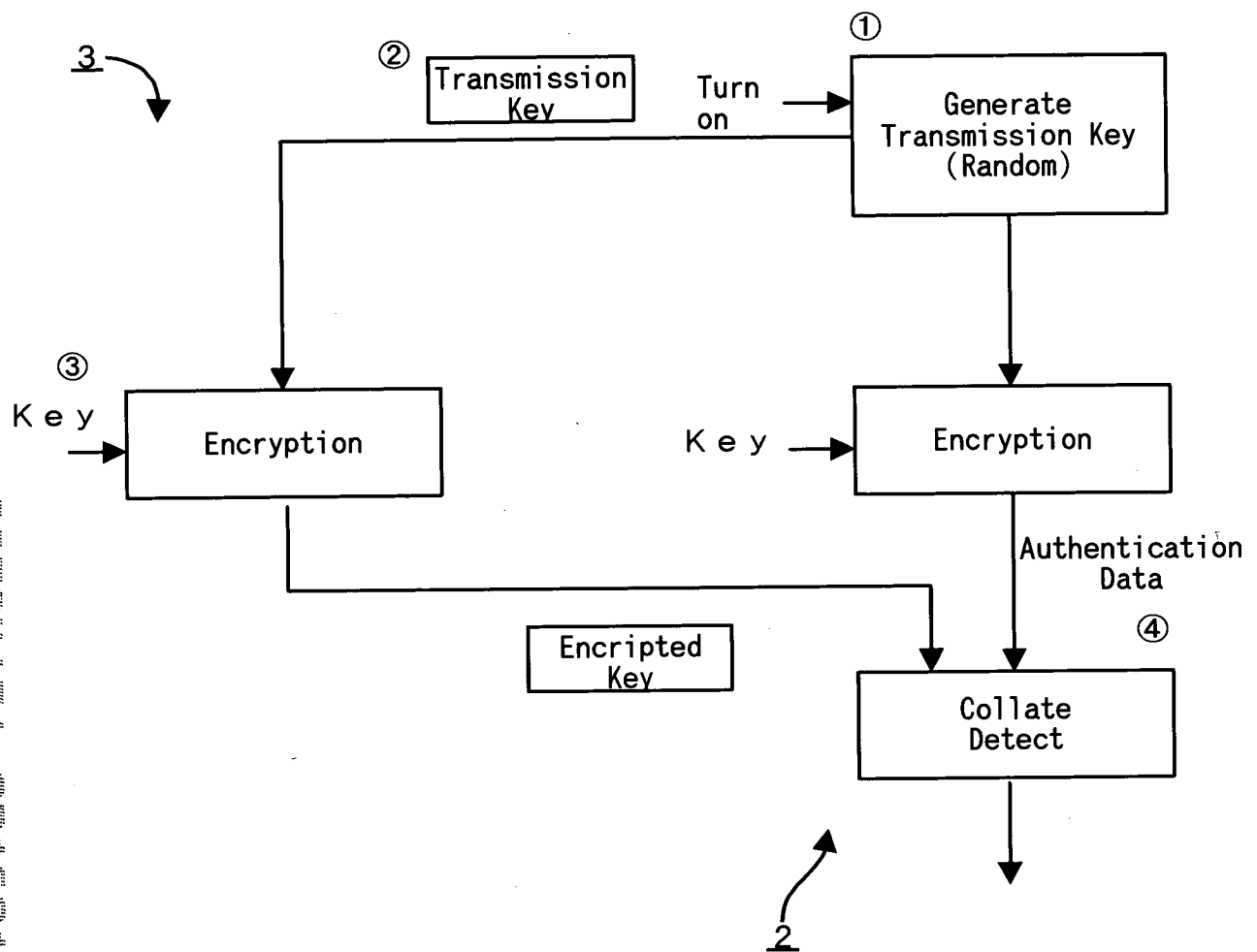
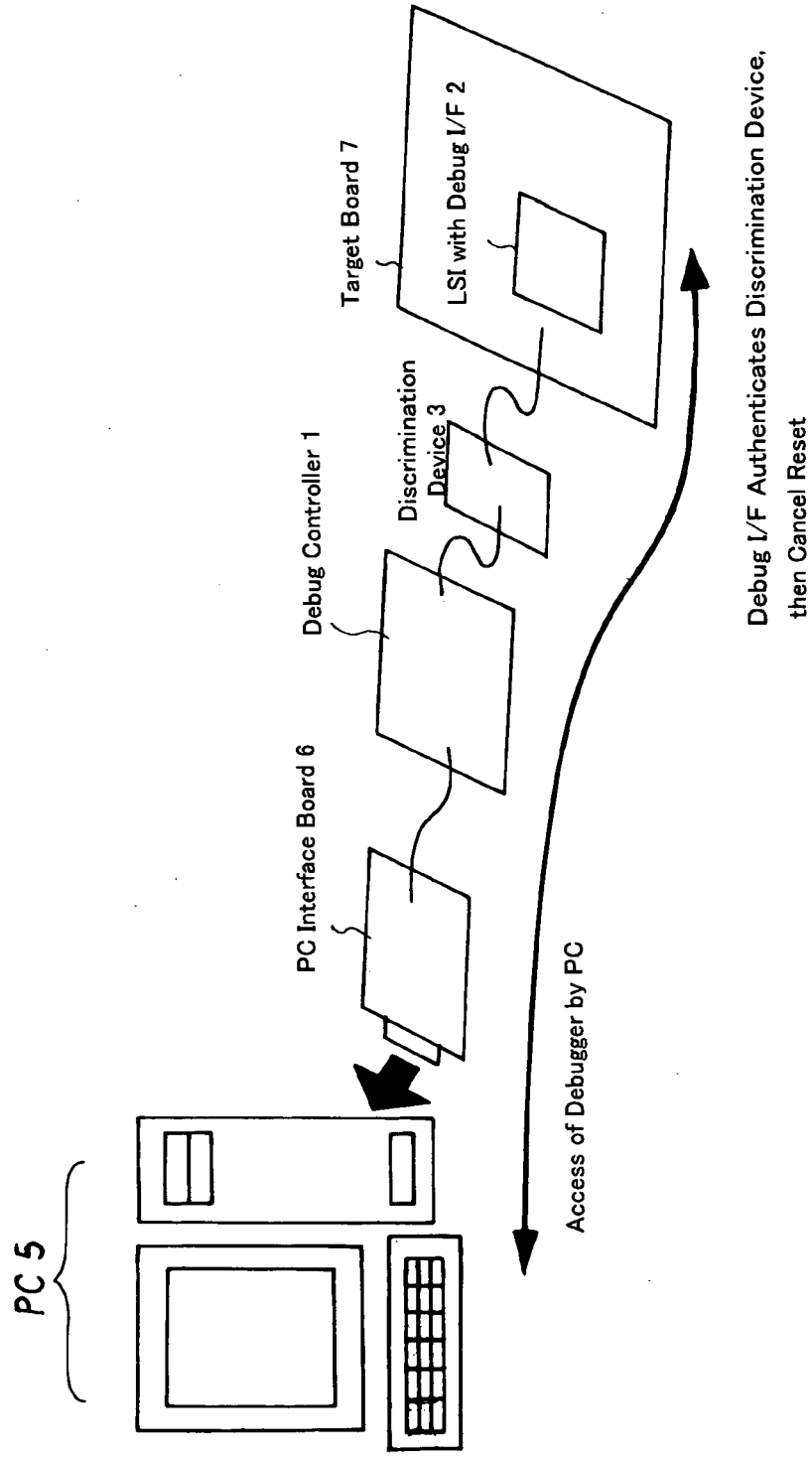


FIG. 3



13 14

FIG. 4

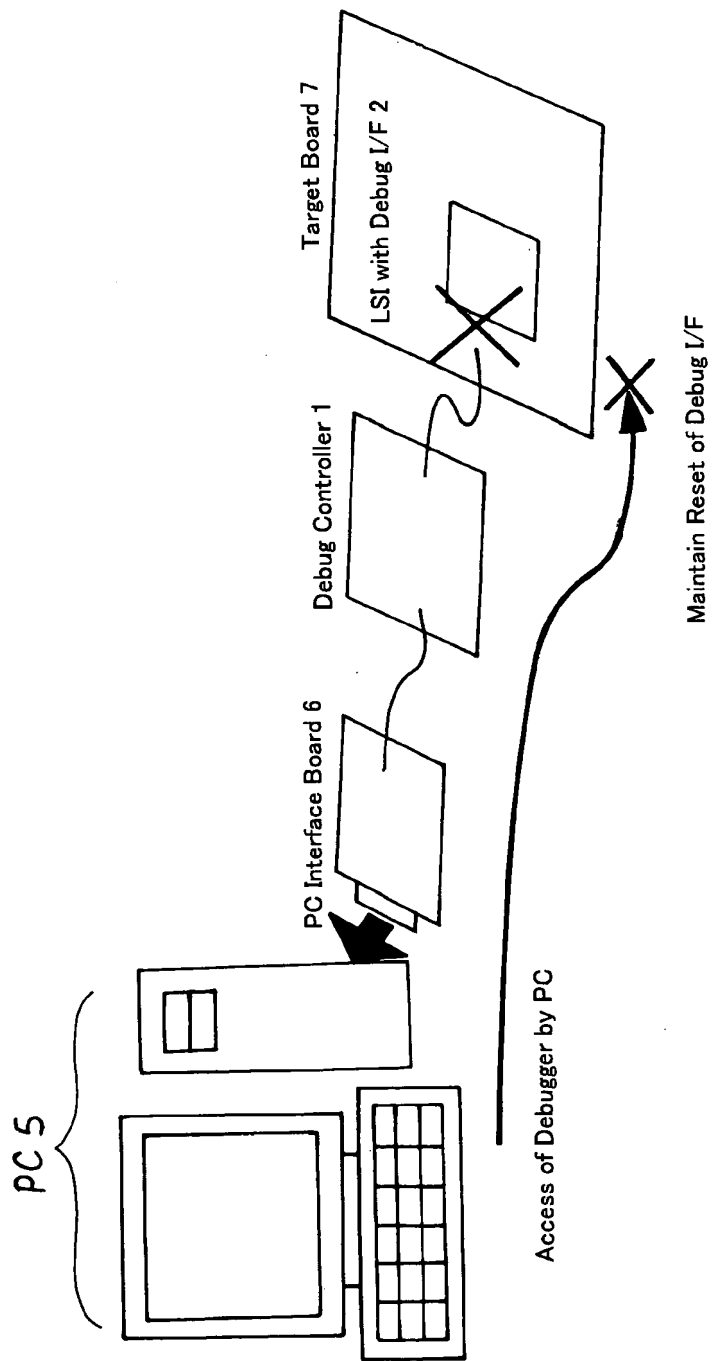


FIG. 5

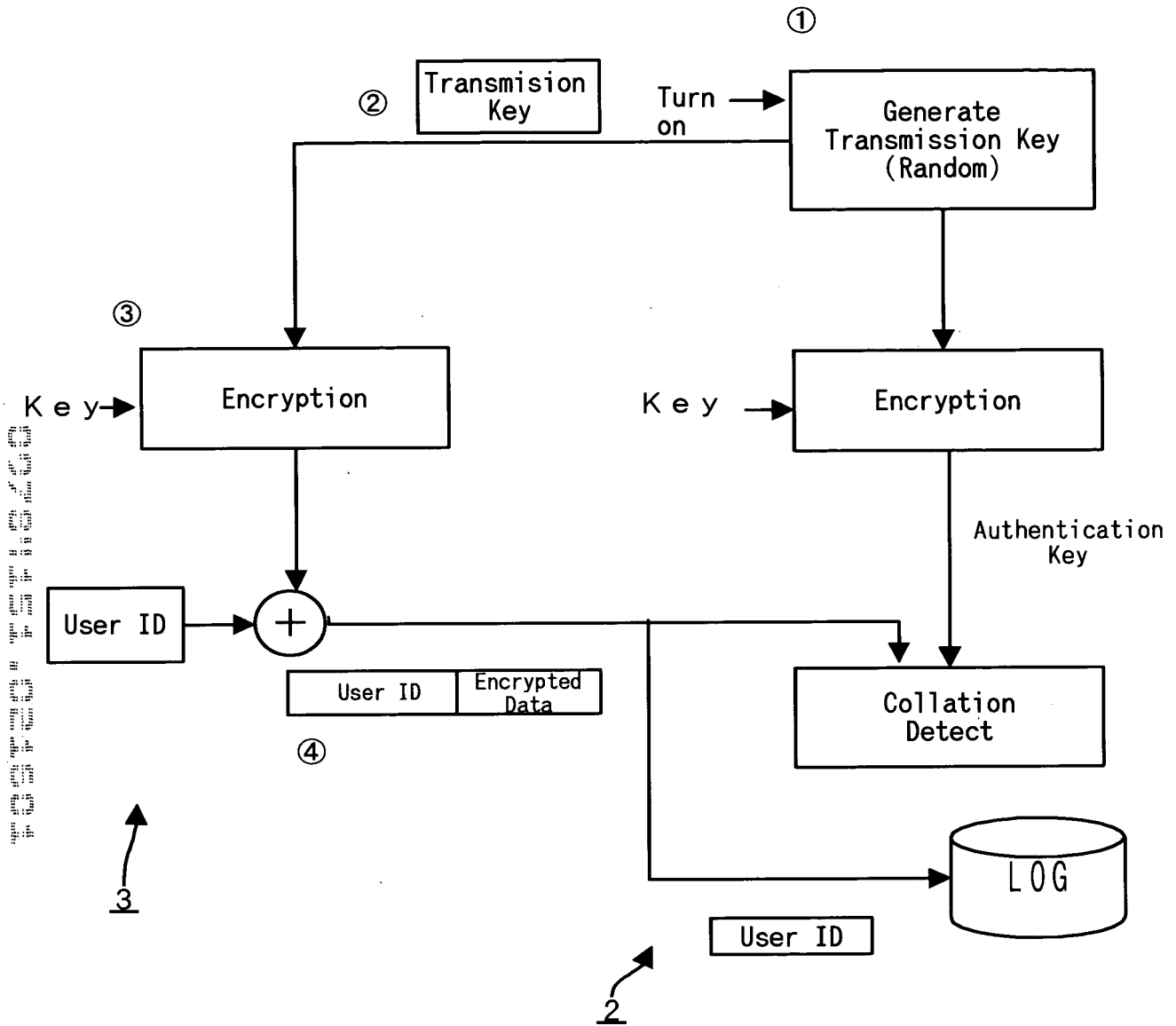


FIG. 6

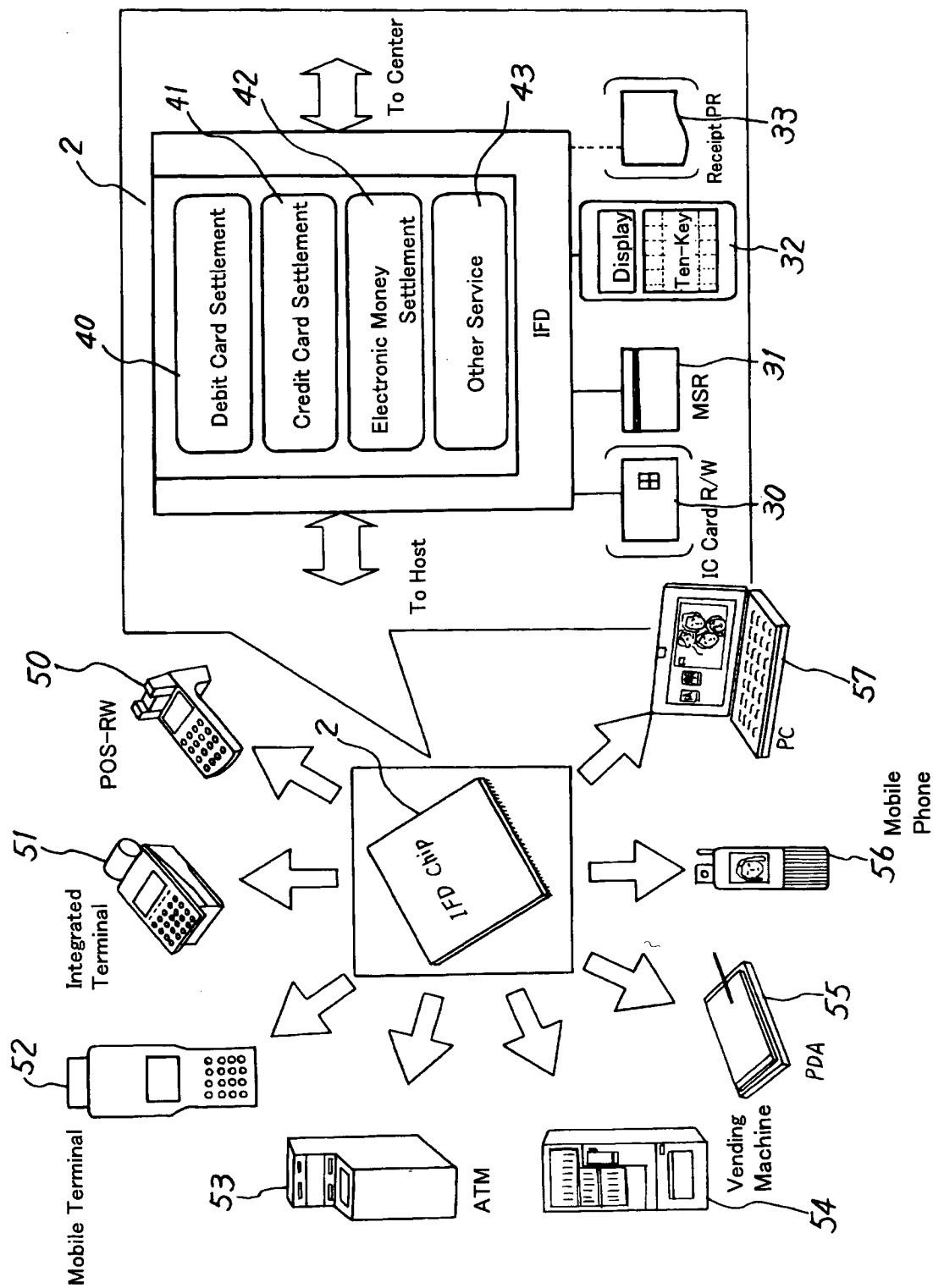


FIG. 7

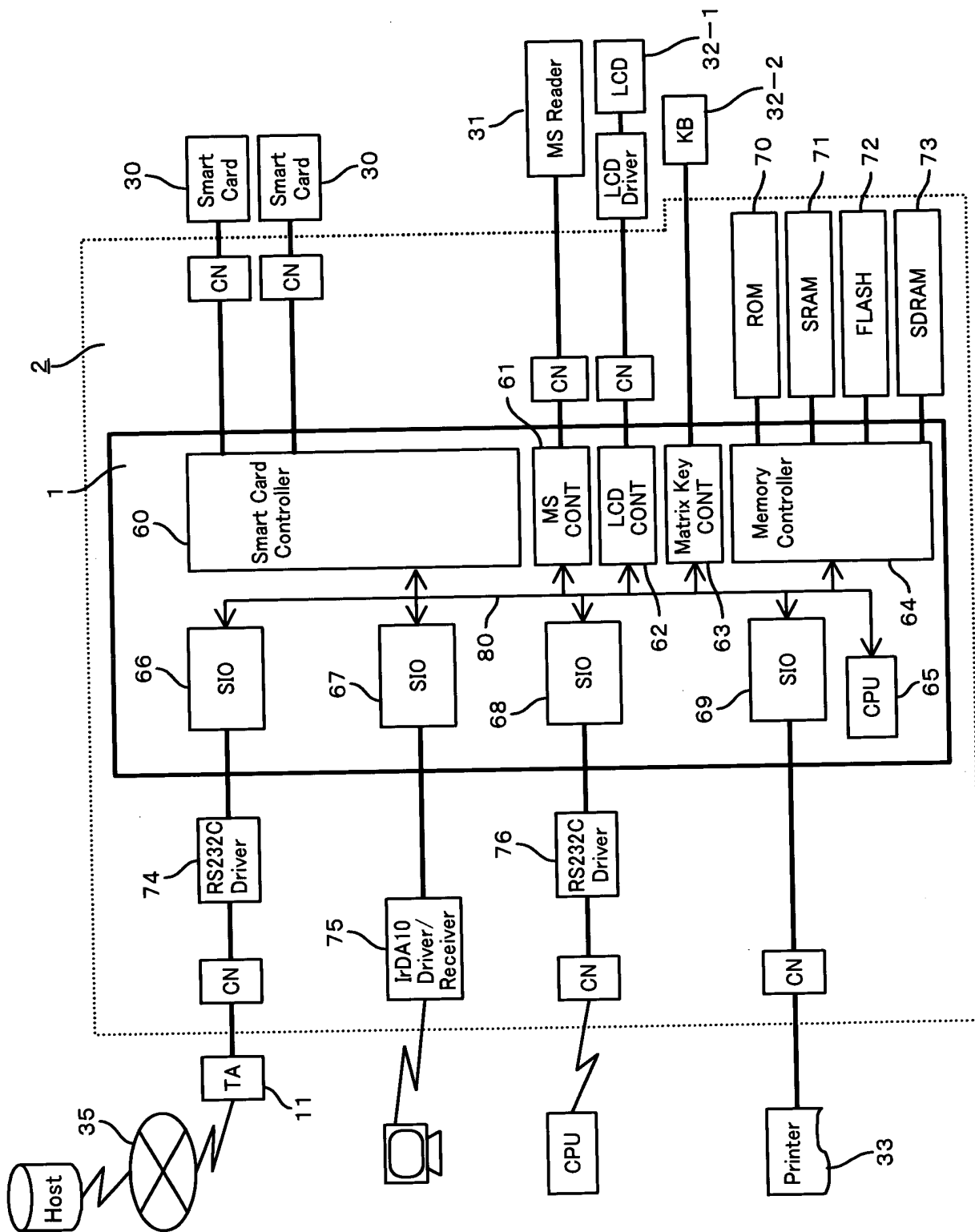


FIG. 8 is a block diagram of a system architecture for a networked environment. The system includes a central network (35) connected to several components. On the left, a POS (10) is connected to the network. In the center, a POS (12) is connected to the network and also to a CPU (13). The CPU (13) is connected to a Terminal Controller (11). The Terminal Controller (11) is connected to an IFD (2) and an ICC (34-2). The IFD (2) is connected to an ICC (34-1). The ICC (34-1) is connected to an ICC R/W (30). The ICC R/W (30) is connected to the network. The network (35) is also connected to a STORE CONTROLLER (20) which includes a CPU (13) and a Terminal Controller (11). The Terminal Controller (11) is connected to an IFD (2) and an ICC (34-2). The IFD (2) is connected to an ICC (34-1). The ICC (34-1) is connected to an ICC R/W (30). The ICC R/W (30) is connected to the network.

FIG. 8

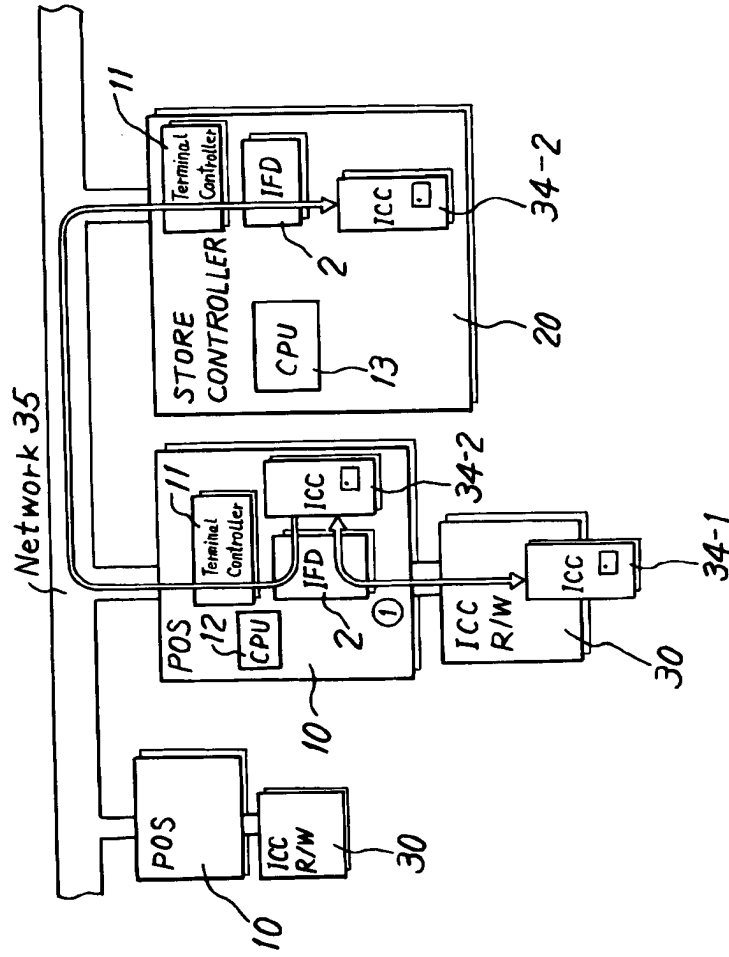




FIG. 9

Prior Art

